CLAIMS

What is claimed is:

1. A memory management apparatus in a video reproducing system, wherein input image data having a format is converted into a suitable format for a display, comprising:

a scaler to convert the format of the input image data;

a first memory having;

an address for writing, at which the format-converted image data is written at a data writing rate, and

an address for reading, from which the format-converted image data is read at a data reading rate; and

a second memory which is substituted for the first memory, wherein the address for reading does not overlap the address for writing, and/or the address for writing does not overlap the address for reading due to a difference between the data reading rate and the data writing rate.

2. The apparatus of claim 1, further comprising a memory controller to control reading and writing operations of the first and second memories.

3. The apparatus of claim 1, further comprising a memory controller to control the substitution of the second memory for the first memory.

4. The apparatus of claim 3, wherein the memory controller is a microprocessor.

5. The apparatus of claim 3, wherein the memory controller calculates a desired address offset between the address for reading and the address for writing in the first memory, using the data reading rate, the data writing rate, and the resolution of the display.

6. The apparatus of claim 3, wherein the memory controller writes the format converted image data, output from the scaler, to the second memory instead of the first memory if a distance between a current address for reading and a current address for writing is within the desired address offset.

7. The apparatus of claim 6, wherein if the reading rate (Dclock) is faster than the writing rate (Mclock) in the first memory, the desired address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) ×
(Dclock - Mclock) / Dclock

8. The apparatus of claim 7, wherein the maximum address of the first memory is calculated by multiplying the resolution of the display by 3.

9. The apparatus of claim 6, wherein if the writing rate (Mclock) is faster than the reading rate (Dclock) in the first memory, the desired address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) ×
(Mclock - Dclock) / Mclock

10. The apparatus of claim 9, wherein the maximum address of the first memory is calculated by multiplying the resolution of the display by 3.

11. A memory management method to prevent image tearing in a video reproducing system comprising:

measuring a data writing rate (Mclock) and a data reading rate (Dclock) of a first memory;

determining an offset distance between a current address for writing and a current address for reading; and

writing image data in a second memory instead of the first memory if the offset distance is within a predetermined address offset.

12. The method of claim 11, wherein if the data writing rate (Mclock) is faster than the data reading rate (Dclock), the predetermined address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) ×
(Mclock - Dclock) / Mclock

13. The method of claim 12, wherein the maximum address of the first memory is calculated by multiplying the resolution of a display on which image data are to be displayed by 3.

14. The method of claim 11, wherein if the reading rate (Dclock) is faster than the writing rate (Mclock) in the first memory, the predetermined address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) × (Dclock - Mclock) / Dclock

15. The method of claim 14, wherein the maximum address of the first memory is calculated by multiplying the resolution of a display on which the image data are to be displayed by 3.

16. A memory management method for preventing image tearing in a video reproducing system comprising:

measuring a data writing rate (Mclock) and a data reading rate (Dclock) of a first memory;

comparing the data writing rate to the data reading rate;

calculating a desired address offset if the data reading rate is faster than the data writing rate;

determining a base address for data reading;

determining a relative address for data writing from the base address for data reading;

determining if a distance between the relative address for data writing and the base address for data reading is greater than or equal to the desired address offset;

if the distance is greater than or equal to the desired address offset, continuing the data writing and the data reading in the first memory; and

if the distance is within the desired address offset, performing the data writing in a second memory instead of the first memory.

17. The method of claim 16, wherein the preferable address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) ×

(Dclock - Mclock) / Dclock

18. The apparatus of claim 17, wherein the maximum address of the first memory is calculated by multiplying the resolution of a display on which image data are to be displayed by 3.

19. A memory management method to prevent image tearing in a video reproducing system comprising:

measuring a data writing rate (Mclock) and a data reading rate (Dclock) of a first memory;

comparing the data writing rate to the data reading rate;

calculating a desired address offset if the data writing rate is faster than the data reading rate;

determining a base address for data writing;

determining a relative address for data reading from the base address for data writing;

determining if a distance between the relative address for data reading and the base address for data writing is greater than or equal to the desired address offset;

if the distance is greater than or equal to the desired address offset, continuing the data writing and the data reading in the first memory; and

if the distance is less than the desired address offset, performing the data writing in a second memory instead of the first memory.

20. The method of claim 19, wherein the base address for data writing is a starting address of the first memory.

21. The method of claim 19, wherein the desired address offset, *Address_offset*, is calculated using the following:

Address_offset = (a maximum address of the first memory) ×

(Mclock - Dclock) / Mclock

22. The method of claim 21, wherein the maximum address of the first memory is calculated by multiplying the resolution of a display on which image data are to be displayed by 3.

23. A computer readable medium on which a program for implementing a method for managing memory to prevent image tearing in a video reproducing system, wherein the method comprises:

measuring a data writing rate (Mclock) and a data reading rate (Dclock) of a first memory;

comparing the data writing rate to the data reading rate;

calculating a desired address offset if the data reading rate is faster than the data writing rate;

determining a base address for data reading;

determining a relative address for data writing from the base address for data reading;

determining if a distance between the relative address for data writing and the base address for data reading is greater than or equal to the desired address offset;

if the distance is greater than or equal to the desired address offset, continuing the data writing and the data reading in the first memory; and

if the distance is within the desired address offset, performing the data writing in a second memory instead of the first memory.

24. The computer readable medium on which a program for implementing a method for managing memory to prevent image tearing in a video reproducing system of claim 23, wherein the computer readable media is distributed to a computer system connected through a network and is stored and executed as a computer readable code in a distributed mode.

25. A computer readable medium on which a program for implementing a method for managing memory to prevent image tearing in a video reproducing system, wherein the method comprises:

measuring a data writing rate (Mclock) and a data reading rate (Dclock) of a first memory;

comparing the data writing rate to the data reading rate;

calculating a desired address offset if the data writing rate is faster than the data reading rate;

determining a base address for data writing;

determining a relative address for data reading from the base address for data writing;

determining if a distance between the relative address for data reading and the base address for data writing is greater than or equal to the desired address offset;

if the distance is greater than or equal to the desired address offset, continuing the data writing and the data reading in the first memory; and

if the distance is less than the desired address offset, performing the data writing in a second memory instead of the first memory.

26. The computer readable medium on which a program for implementing a method for managing memory to prevent image tearing in a video reproducing system of claim 25, wherein the computer readable medium is distributed to a computer system connected through a network and is stored and executed as a computer readable code in a distributed mode.